IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect cancellation of claims 20, 21, 24, 28 and 30, amendment of previously pending claims 17, 18, 22, 23, 25, 26, 27, 31-36 and 40, and addition of new claims 41-50. The specific amendments to individual claims are detailed in the following marked up set of claims.

17. (Once Amended) A memory cell, comprising:

a lateral transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region;

a trench capacitor formed in a trench and coupled to the first source/drain region; and

[wherein the trench capacitor includes] a first plate of polycrystalline material formed in the trench that is coupled to a second plate integral with the first source/drain region thereby forming a conductorless electrical connection between the trench capacitor and the transistor, [a] the second plate [formed by the substrate with a surface of the substrate in the trench] having an etch-roughened surface [roughened by etching a polycrystalline semiconductor material on the surface of the substrate,] ; and

an insulator layer that separates the first polycrystalline [semiconductor] plate from the etch-roughened surface of the [substrate] second plate.

18. (Once Amended) The memory cell of claim 17, wherein the first polycrystalline semiconductor plate comprises polysilicon.

22. (Once Amended) A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned;

wherein a surface of the first source/drain region [is] includes integral therewith a first polycrystalline plate having a polycrystalline surface layer that is etch-roughened [by etching a

polycrystalline semiconductor material on a surface of the first source/drain region]; [and]

a trench capacitor [with] having a second plate that is formed in a trench that surrounds the [roughened surface of the first source/drain region of the transistor] first plate;[.] and

wherein the first plate forms a conductorless electrical connection between the trench capacitor and the transistor.

23. (Once Amended) The memory cell of claim 22, wherein the first plate integral with the first source/drain region comprises single crystalline silicon upon which is formed [with] a layer of polysilicon [formed on its surface in the trench, wherein the layer of polysilicon includes a phosphoric-acid-etch-roughened surface].

25. (Amended) The memory cell of claim 22, wherein the second plate comprises polysilicon.

26. (Once Amended) A memory device, comprising:

an array of memory cells, each memory cell including an access transistor that is coupled to a trench capacitor wherein a first plate of the trench capacitor is integral with a first source/drain region so as to form a conductorless electrical connection between the trench capacitor and the access transistor, the first plate including [includes] a micro-roughened surface layer of porous polysilicon, and a second plate of the trench capacitor disposed adjacent to the first plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at a [first] second source/drain region of the access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

27. (Once Amended) The memory device of claim 26, wherein the first plate comprises a single crystalline layer upon which is formed the layer of polysilicon [formed on a surface in the trench and includes a phosphoric-acid-etch-roughened surface].

31. (Once Amended) A memory cell, comprising:

a lateral transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region having a first plate formed integral therewith, a body region and a second source/drain region; and

a trench capacitor formed in a trench and electrically coupled without an intervening conductor to the [first source/drain region] first plate;

wherein the trench capacitor includes a polysilicon plate formed in the trench that is coupled to the first plate of the first source/drain region, [a second plate formed by the substrate with a surface of the substrate in the trench] the first plate including a surface layer of polysilicon that is etch- roughened [by etching a polysilicon material on the surface of the substrate], and an insulator layer that separates the second polysilicon plate from the etch-roughened polysilicon surface of the first plate [substrate].

32. (Once Amended) The memory cell of claim 31, wherein the [second] first plate comprises [a] heavily doped p-type silicon [substrate].

33. (Once Amended) A memory cell, comprising:

a lateral transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region having a first plate formed integral therewith, a body region and a second source/drain region; and

a trench capacitor formed in a trench and electrically coupled without an intervening conductor to the [first source/drain region] first plate;

wherein the trench capacitor includes a second plate of polysilicon [plate] formed in the trench [that is coupled to] so as to surround the first plate [first source/drain region, a second plate formed by the substrate in the trench, the second plate having a phosphoric-acid-etch-

roughened surface or an anodic-etch-roughened surface], and an insulator layer that separates the second polysilicon plate from at least the [phosphoric-acid-] etch-roughened surface [or anodic-acid-etch-roughened surface] of the [substrate] first plate.

34. (Once Amended) A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned, wherein the first source/drain region [comprises] includes integral therewith a single crystalline silicon first plate with a layer of polysilicon [formed on its] having an etch-roughened surface; and

a trench capacitor with a second plate that is formed in a trench and that surrounds [a] at least the etch-roughened surface of the [first source/drain region of the transistor] first plate; and

wherein the first plate forms a conductorless electrical connection between the trench capacitor and the transistor.

35. (Once Amended) A memory device, comprising:

an array of memory cells, each memory cell including an access transistor that is electrically connected without an intervening conductor [coupled] to a trench capacitor [wherein] by a first plate of the trench capacitor that is integral with a first source/drain region of the access transistor, the first plate including [includes] a micro-roughened surface of porous polysilicon , with a second plate of the trench capacitor [is] disposed [adjacent] so as to surround [to] at least the micro-roughened surface of the first plate [further wherein the micro-roughened surface of porous polysilicon is anodic-etch-roughened or phosphoric-acid-etch-roughened];

a number of bit lines that are each selectively coupled to a number of the memory cells at a [first] second source/drain region of the access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

36. (Once Amended) The memory device of claim 35, wherein the access transistor comprises a lateral transistor [that is coupled to the second plate of the trench capacitor].

40. (Once Amended) The memory cell according to claim 35, wherein the [portion] first source/drain of the access transistor is P-doped or N-doped.

41. (New) A memory cell, comprising:

a lateral transistor comprising outwardly from a substrate a first source/drain region at least a portion of which serves as a single crystalline first capacitor plate for forming a conductorless connection of the transistor to a trench capacitor, a body region and a second source/drain region, wherein the first capacitor plate includes a micro-roughened surface for increasing the capacitance of the trench capacitor;

the trench capacitor being formed in a trench surrounding a portion of the lateral transistor and including a second capacitor plate of polycrystalline material formed so as to surround the first capacitor; and

an insulator layer that separates the second polycrystalline semiconductor plate from the micro-roughened surface of the first plate.

42. (New)A memory cell according to claim 41, wherein the micro-roughened surface of the first capacitor plate comprises a layer of polysilicon.

43. (New) A memory cell according to claim 41, wherein the first source/drain that includes the first capacitor plate, the body region, and the second source/drain region are formed as a pillar of single-crystal semiconductor material.

44. (New) A memory cell according to claim 41, wherein the second plate also surrounds first plates of adjacent memory cells.

45. (New) A memory cell according to claim 44, wherein the second plate is grounded.

46. (New) A memory cell according to claim 17, wherein the first plate also surrounds second plates of adjacent memory cells.

47. (New) A memory cell according to claim 26, wherein the second plate also surrounds first plates of adjacent memory cells.

48. (New) A memory cell according to claim 31, wherein the second plate also surrounds first plates of adjacent memory cells.

49. (New) A memory cell according to claim 33, wherein the second plate also surrounds first plates of adjacent memory cells.

50. (New) A memory cell according to claim 35, wherein the second plate also surrounds first plates of adjacent memory cells.

REMARKS

In the Specification

The specification has been amended to correct a mistaken reference to "pillars 104A through 104D." The pillars are labeled as 104, while the memory cells containing pillars 104 are labeled as 102A through 102D.

In the Claims

Applicant has carefully reviewed and considered the Office Action mailed on June 5, 2001, and the references cited therewith.

Claims 17, 18, 22, 23, 25, 26, 27, 31-36 and 40 are amended, claims 20, 21, 24, 28 and 30 are canceled, and claims 41-50 are added; as a result, claims 17, 18, 19, 22, 23, 25, 26, 27, 29, 31- 50 are now pending in this application.